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10/069,306	07/03/2002	Donald F. Hooper	10559-303US1	1999

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,306	HOOPER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,11,15-20 and 22-25* is/are rejected.

7)☒ Claim(s) *6,7,9,10,12-14 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/03/02* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/04/04, 02/21/02*. 12/06/04, 12/12/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-25 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 ,15,16,20,22,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moller (4768135) in view of Bitar (5,872,963).

3. As to claims 1 ,15,16,20,22,24, Moller disclosed a system including at least a swap instruction (swap microinstruction) that swaps a currently running context, corresponding to a first loop (see invoking loop) in a specified microengine (see fig.2A,B) to let another context (invoked loop counter) to execute in that microengine and causes a different context (invoked loop counter), corresponding to different loop (invoked loop) and associated program counter to be selected (see the selection, the downloaded loop counter, and the replacement of the invoked loop count in the stack for execution in col.30, lines 39-54).

Moller also taught at least :

a) evaluating the state of a parameter of context process corresponding to a first loop (see the generation of CMUXCTL and STKMUXCTL in col.30, lines 39-54, see the invoking loop);

b) performing swapping to cause a different context (invoked loop) and associated

Program Counter, corresponding to different loop (invoked loop count) , to be Selected in accordance with the parameter (see the selection, the download, and the replacement of the invoked loop count for execution in col.30, lines 39-54).,

c) register stack (see the stack in col.30, lines 39-54, fig.2A (stack));

d) arithmetic unit coupled to the register stack and a program control store for string the context swap instruction (see the ALU and program counter and memory and the microprogramming sequencer 10 in fig.1).

4. As far as the parallel multithreaded processor in preamble, since no specific structure of the multithread has been reflected into the claim, it is read as any software construct in general, such as a nested loop, or a nested subprogram.

5. As to the microengine in claim 1, although in applicant's specification (pages , lines 28-33) teaches the microengines maintain the program counter in hardware, it also taught in page 3, lines 14-16, that the microengines can execute memory reference instructions to access the RAMS, and the sram SWAP (see claim 4) is the parameter field of a swap instruction (page 19, lines 1-1 1). The hardware structure of the micro engines are not being reflected into the claim. Therefore, the microengine is read as any functional element to swap the context in either hardware or instruction format in general.

6. Moller did not specifically teach the use of the threads as claimed. Instead , Moller taught the use of loops. However, Bitar disclosed that a suitable number of threads were used to execute a loop in parallel (see col.10, lines 51-59). Therefore, it

would have been obvious to one of ordinary skill in the art to use Bitar in Moller for including the threads as claimed because the use of Bitar could provide Moller the ability of the system to adapt to specific processing structure at a predefined set of software constructs (e.g. threads), and thereby, minimizing the overall latency of the loop processing in Moller, and because Moller also taught his system was used as building blocks in an architecture divided in control subsections (see col.1, lines 24-35), which was a suggestion of the need for providing subdivided control programs for specific subsections of the system, and therefore, one of ordinary skill in the art should be able to recognize the use of threads as taught by Bitar into Moller in order to achieve the enhanced processing cycle, and in doing so, provided a motivation.

7. As to claim 20, Moller also included an inter thread (see inner loop in col.30, lines 25-54).

8. Claims 2 ,3,8, 17, 23, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar (5,872,963) as applied to claims 1,15,22,24 above,, and further in view of Adkins (5,247,671).

9. As to claim 2,23, 25, limitations of parent claims 1,15,22,24 have been discussed in previous paragraphs, therefore, they are not repeated herein. Neither Moller nor Bitar specifically showed the wakeup of the swap out context as claimed. However, Adkins disclosed a wakeup of a context (see col.8, lines 45-64). It would have been obvious to one of ordinary skill in the art to use Adkins in Moller for including the wakeup of the swapped context as claimed because the use of Adkins could provide Moller the control ability to restore the context of the associated task at a predetermined cycle, thereby reducing the latency caused during the resume of the task process, and it could be readily achieved by predefining the wakeup signals of Adkins into the swap instructions of Moller with modified read and write operands so that the specific wakeup command of the context of a given task of Adkins could be recognized by Moller, and because Moller did teach the activation of the context on the top of a stack by a selection signal caused by the swap instruction (see col.30, lines 39-44), which was a suggestion of the need of a function specific signal (e.g. wakeup, sleep, etc) into the swap instruction in order to achieve the enhanced context recovery or activation, and for the above reasons , provided a motivation. Moller is used as a primary reference because it clearly showed a swap instruction (see swap instruction) in col.30, lines 39-40). Adkins is used as secondary because it supplemented the teaching of the wakeup of the context.

10. As to claims 3,17, Moller did not specifically show the specifying of an occurrence in the instruction as claimed. However, Adkins disclosed context wakeup in response to new event (see col.8, lines 47-52). It would have been obvious to one of

ordinary skill in the art to use Adkins for including the occurrence of event because the use of Adkins could provide Moller the control ability to restore the context of the associated event at a given command, therefore eliminating the hardware overheads during the resume of the task process.

11. As to claim 8, Moller was also directed to a inter-thread (see the inner loop in col.30, lines 25-68, col.31 , lines 1-5).

12. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar (5,872,963) as applied to claim 1 above, and further in view of Adkins (5,247,671) as applied to claim 3 above, and further in view of Angle (5,541 ,920).

13. As to claims 4, Neither Moller nor Bitar nor Akins specifically showed the sram swap signal as claimed. However, Angle taught a sram swap signal for swapping the portion of the SRAM (see col.5, lines 1-8) . It would have been obvious to one o f ordinary skill in the art o use Angle in Moller for including sram swap signal as claimed because the use of Angle could provide additional option of the swap instruction in Moller , and therefore, expanding the processing capability for accepting different memory type such as the SRAM.

14. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar (5,872,963) as applied to claim 15 above, and further in view of Angle (5,541 ,920).

15. As to claims 18, Neither Moller nor Bitar specifically showed the sram swap signal as claimed. However, Angle taught a sram swap signal for swapping the portion of the SRAM (see col.5, lines 1-8) . It would have been obvious to one o f ordinary skill in the art o use Angle in Moller for including sram swap signal as claimed because the use of Angle could provide additional option of the swap instruction in Moller , and therefore, expanding the processing capability for accepting different memory type such as the SRAM.

16. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar as applied to claim 1, and further in view of Adkins (5,247,671) as applied to claim 3 above, and further in view of Manning (5,610,864).

17. AS to claim 5, Neither Moller nor Bitar, nor Adkins specifically showed the swap of sdram as claimed . However, Manning disclosed a background art which taught a swapping of the SRAM and DRAM (see OTHER PUBLICATIONS, Page 2, lines 1-5). Since no specific format of the swap of the SRAM and DRAM has been reflected into the claim , it is assumed to be a swapping of the SRAM and DRAM in general sense. For example, DRAM can be swapped for SRAM. As to the swapping of the SRAM and DRAM, it would have been obvious to one of ordinary skill in the art to use Manning in Moller for including the swap of the SRAM and DRAM

because the use of Manning could enhance the adaptability of Moller for accepting different type of memory, such as DRAM and SRAM. Manning is used because it was built based on the background art including the publication teaching of the swap of the DRAM for SRAM. No details of the publication has been used and cited to applicant because no specific format of the swap signal has been reflected into the claim. The idea of DRAM can be swapped for SRAM was already set forth clearly in the title of the publication, and one of ordinary skill in the art should be able to implement the swapping into Moller's swap instruction to achieve the storage access flexibility.

18. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar as applied to claim 15, and further in view of Manning (5,610,864).

19. AS to claim 19, neither Moller nor Bitar, nor Adkins specifically showed the swap of sdram as claimed . However, Manning disclosed a background art which taught a swapping of the SRAM and DRAM (see OTHER PUBLICATIONS, Page 2, lines 1-5). Since no specific format of the swap of the SRAM and DRAM has been reflected into the claim , it is assumed to be a swapping of the SRAM and DRAM in general sense. For example, DRAM can be swapped for SRAM. As to the swapping of the SRAM and DRAM, it would have been obvious to one of ordinary skill in the art to use Manning in Moller for including ht swap of the SRAM and DRAM the use of Manning could enhance the adaptability of Moller for accepting because different type of memory such as DRAM and SRAM. Manning is used because it was built based on the background art including the publication teaching of the swap of the DRAM for SRAM. No details of

the publication has been used and cited to applicant because no specific format of the swap signal has been reflected into the claim. The idea of DRAM can be swapped for SRAM was already set forth clearly in the title of the publication, and one of ordinary skill in the art should be able to implement the swapping into Moller's swap instruction to achieve the storage access flexibility.

20. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (4,868,735) in view of Bitar (5,872,963) as applied to claim 1, and further in view of Adkins (5,247,671) as applied to claim 3 above, and further in view of Turner et al. (6,505,229).

15. As to claim 11 , neither Moller nor Adkins specifically showed the available data in the receive FIFO as claimed. However, Turner disclosed a system including a ready FIFO queue for allowing a swapping for a thread (see col.7, lines 38-37). It would have been obvious to one of ordinary skill in the ad to use Turner in Moller for including the available data in FIFO as claimed because the use of Turner could provide additional capability of the given swap command to initiate the swapping at the available cycle of the FIFO , therefore, minimizing the wait time in the access cycle, and it could be readily done by configuring the FIFO of Turner with modified interface ports into Moller so that the available data in FIFO of Turner could be recognized by Moller, and for the above reasons , provided a motivation.

21. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the FBI swapping and wakeup when the thread's FBI was received indicating the FBI CSR, Scratchpad, TFIFO, or RFIFO has completed.

22. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the parameter "seq_num1 change/seq-num2 change" which specifies swap out of the current context and wakes it up when the value of the sequence number changes.

23. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior ad of record further teaches the voluntary parameter for swapping out if another thread is ready to run, and if the thread is swapped , the swapped thread is automatically re-enabled to run at some subsequent context arbitration point.

24. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the auto-push for swapping out and wakes up when SRAM transfer read register data has been automatically pushed by Fbus interface.

25. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the parameter specifying kill for preventing the current context or thread from executing again until the appropriate enable bit for the thread is set in the CTX ENABLES register.

26. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior ad of record further teaches the pci parameter for swapping out and wakes up when the PCI unit signals a DMA transfer has been completed.

27. Claims 14 , 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the optional _token "defer one" for specifying that one instruction will be executed after this reference before the context is swapped.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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